HARI.233US0
(1 of 4)

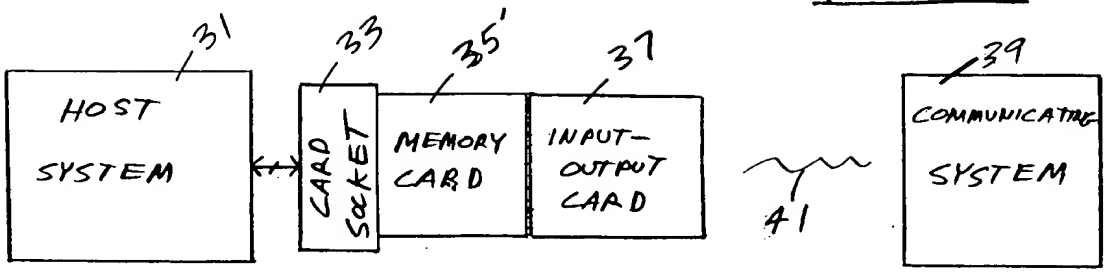


FIG. 1

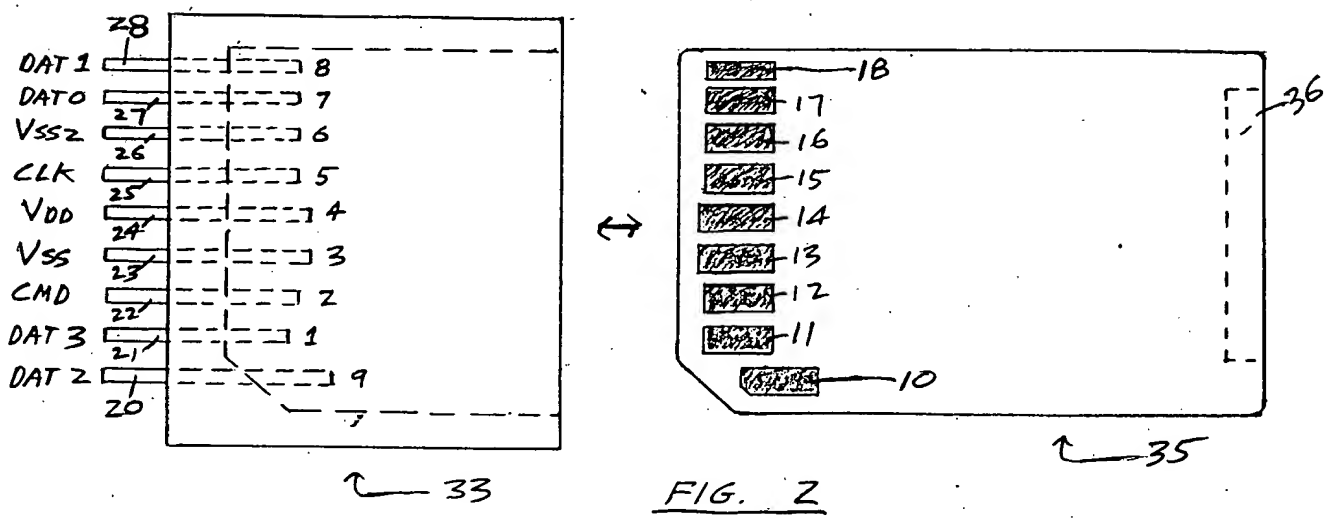


FIG. 2

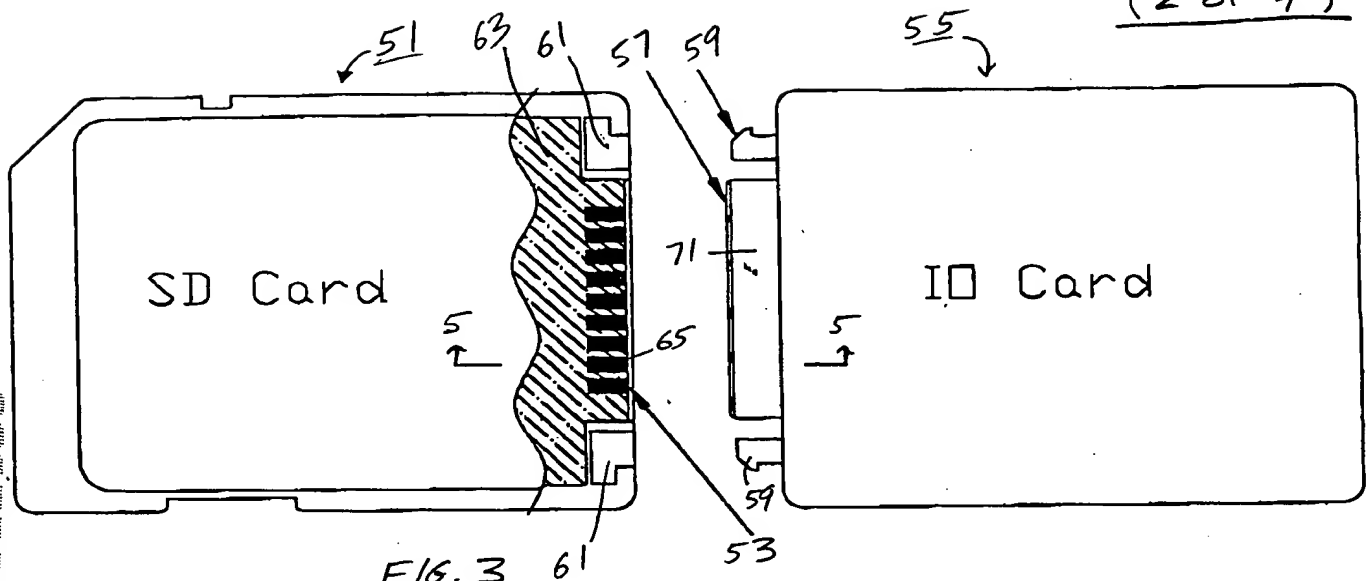


FIG. 3

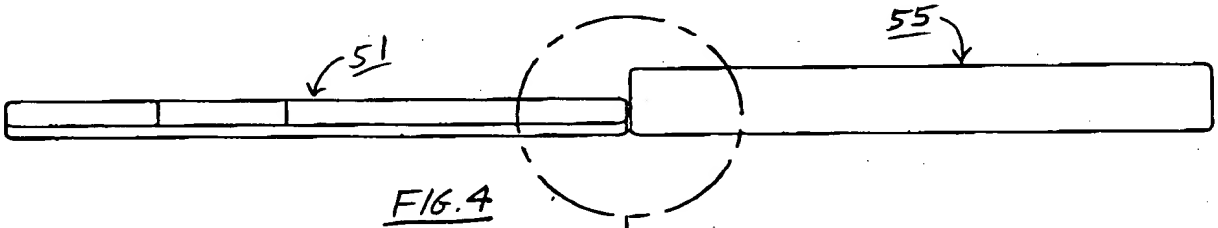


FIG. 4

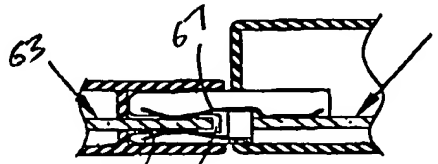


FIG. 5A

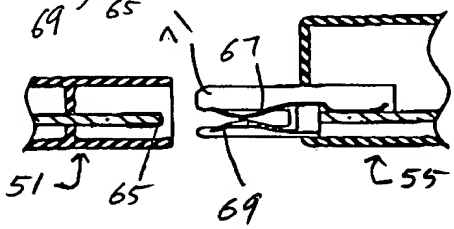


FIG. 5B

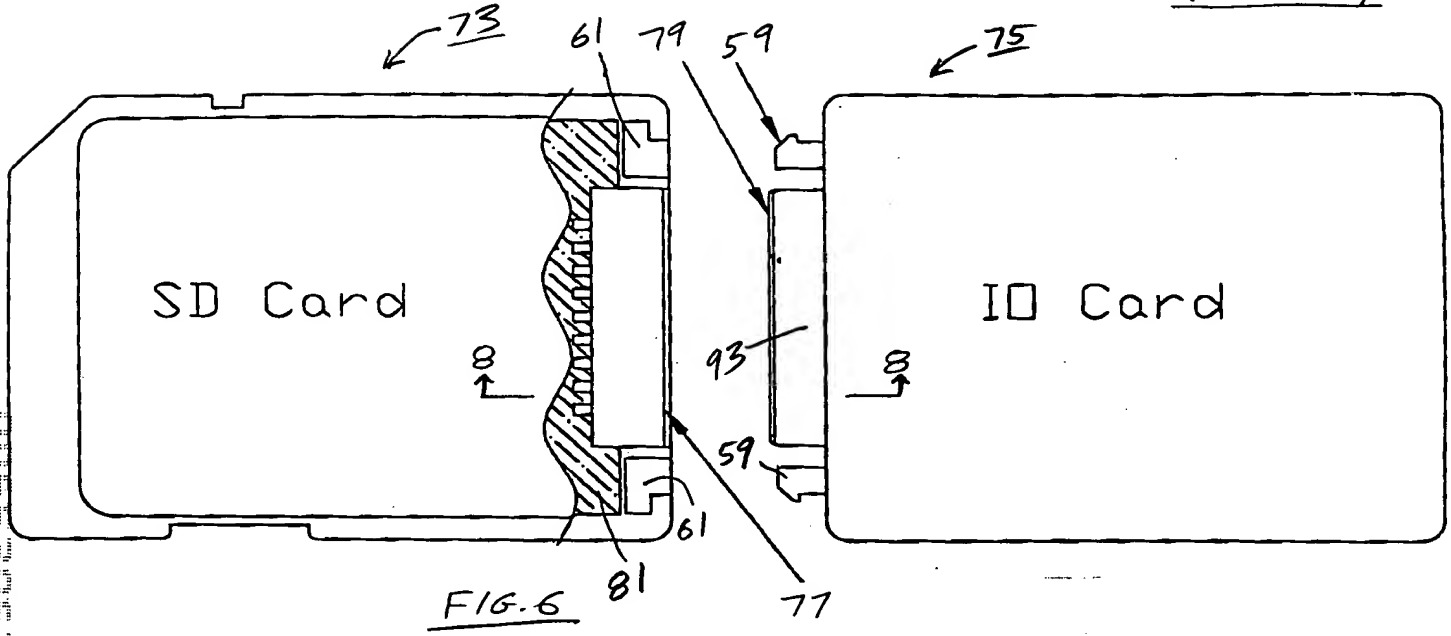


FIG. 6

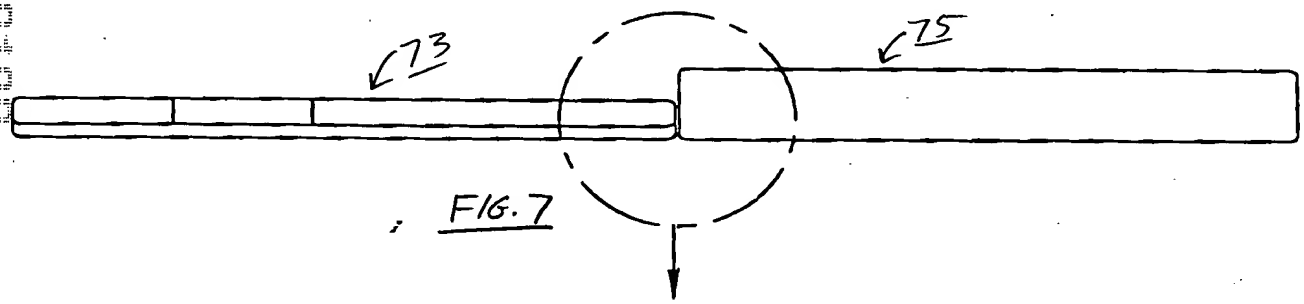


FIG. 7

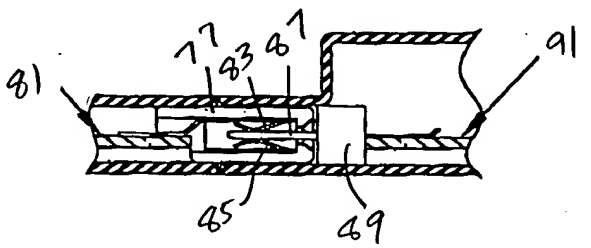


FIG. 8A

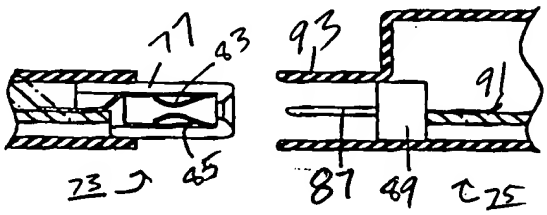


Fig. 8B

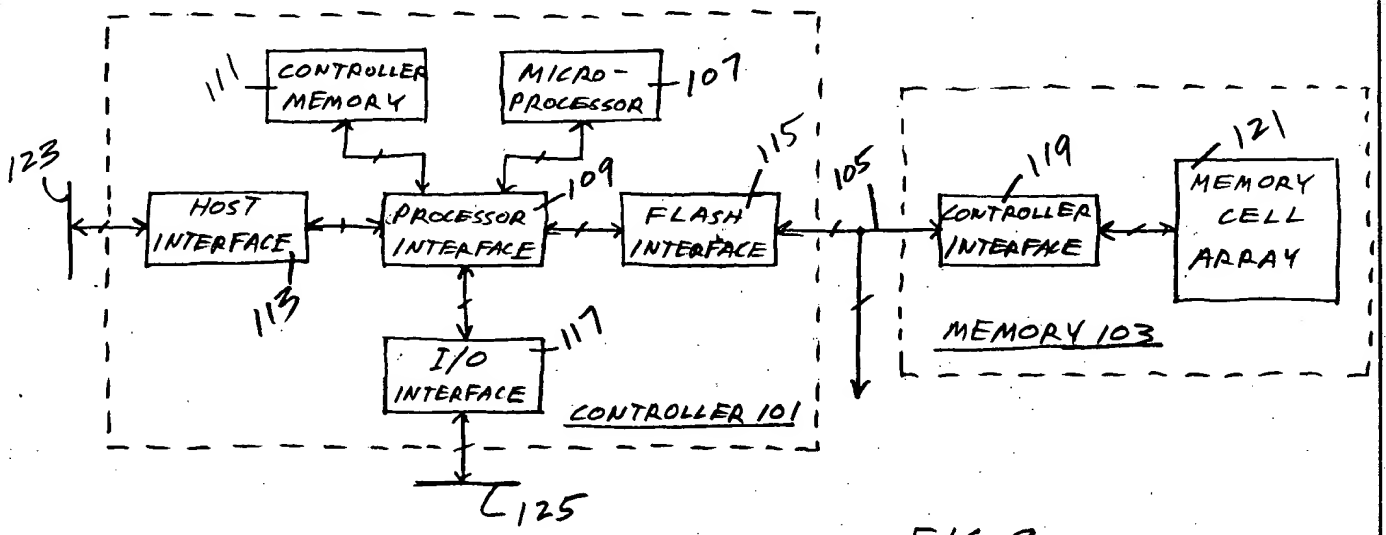
111
CONTROLLER MEMORY
MICRO-PROCESSOR
107
123
HOST INTERFACE
PROCESSOR INTERFACE
109
FLASH INTERFACE
115
105
119
CONTROLLER INTERFACE
121
MEMORY CELL ARRAY
113
I/O INTERFACE
117
MEMORY 103
CONTROLLER 101
125

FIG. 9

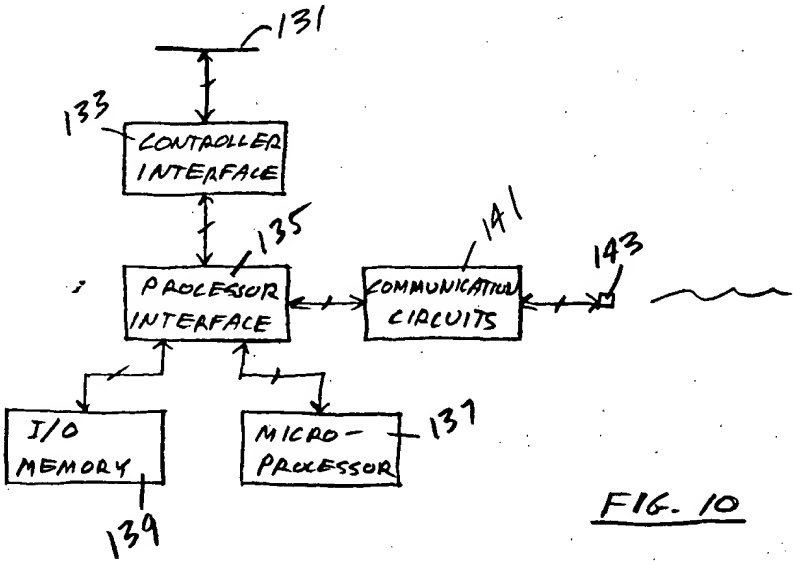
131
133
CONTROLLER INTERFACE
135
PROCESSOR INTERFACE
141
COMMUNICATION CIRCUITS
143
I/O MEMORY
139
MICRO-PROCESSOR
137

FIG. 10